National Nano Fabrication Centre (NNFC)

Tool and Process Capabilities

1. Lithography

1.1 Direct Laser Writer/Lithography

1.1.1 Preferred Design file format: GDS2 or CIF

1.1.2 Please note that coloured portion on your design will be transparent on the mask

1.1.3 Mask fabrication up to 5 inch in size (we have 3,4 & 5 inch masks in stock) Eg. For 5 inch mask size(square), active writing area is 4” diameter circle

1.1.4 Direct writing on the Substrates can also be done, of sample size 1cm x 1cm to 4” wafer

1.1.5 Minimum feature of 3um (3um size, 3um space dense patterns can be made on upto 5inch mask).

1.1.6 On 200umx200um area with a gap of upto 1.5 um between large features can be made

1.2 eBeam Lithography

1.2.1 Minimum sample size of 1cmx1cm is required for processing

1.2.2 Maximum writing area is 6mmx6mm with dense patterns

1.2.3 Substrate Material preferred is Silicon or Thin oxide

1.2.4 Larger area writing is discouraged due to exorbitantly long durations

1.2.5 Minimum feature of 50nm (critical dimension 50nm with a minimum gap of 50nm can be made)

1.3 Photo Lithography/UV Exposure

1.3.1 Wide variety of Positive and Negative Photo resists including SU8 series

1.3.2 Minimum feature of 3um

1.3.3 With a commercially available quartz mask and deep UV lithography minimum feature of upto 1um can be realized

1.3.4 Top side alignment accuracy of 2um and Bottom Side Alignment Accuracy of 3 um can be acheived

1.3.5 MJB4 – Alignment Topside 1um (full wafer) /bottom side 5um (double-side polished 2inch wafer)

1.3.6 EVG – Alignment Topside - 1um (full wafer)/ bottom side 3um (full wafer)

1.4 Wafer Bonder

1.4.1 Wafer/ Substrate Parameter : Up to 4 inch diameter Substrate and small wafer pieces upto 1cmx1cm can be handled

1.4.2 Types of bonding Available:

1.4.2.1 Eutectic bonding (Si-Au-Si)

1.4.2.2 Anodic bonding (Si-Glass)

1.4.2.3 Fusion bonding

1.4.2.4 SU8 bonding is possible

1.4.3 Bond temperatures up to 450°C

2. Deposition

2.1 CVD

2.1.1 **LPCVD**: Si3N4 (Low stress ~400MPa for 800nm, High stress ~1.2GPa for 200nm),

2.1.2 Poly Silicon (Undoped, P, N Type doped), thickness range 40nm to 500nm

2.1.3 Amorphous Silicon (Undoped, P, N Type doped), thickness range 40nm to 200nm

2.1.4 Germanium and Silicon Germanium (Undoped, P, N Type doped), thickness range 40nm to 200nm

2.1.5 Low Temperature SiO2, TEOS (Undoped, P, N Type doped),thickness range 30nm to 500nm(LTO*,TEOS), LTO >100nm, 10% uniformity,

2.1.6 Si Nanowire growth (Au as seed layer),
2.1.7 LPCVD furnace maximum temperature of upto 850C
2.1.8 **Furnaces**: Dry Oxidation 5 to 100nm
2.1.9 Wet Oxidation 300nm to 1000nm
2.1.10 Phosphorous doping and Boron Doping in Silicon
2.1.11 Maximum temperature of upto 1050C for furnace
2.1.12 Annealing (Forming Gas ,O_2 , N_2) and Rapid Thermal Processing Temperature of upto 1050 C, Substrate Size from Small pieces to a single4 ” full wafer, Ramp rates from 20 deg C/s to 200 deg C/s, SiO2 thickness 5 to 30nm(RTP2)
2.1.13 **PECVD**: SiNx, Amorphous Si, SiO_2, SiO_xN_y, Ge, SiGe,
2.1.14 Temperature of upto 350C
2.1.15 Post processing required for converting amorphous films to poly films
2.1.16 Substrate size of 1cmx1cm to 4” wafers
2.1.17 Substrate types: silicon,glass,sapphire (other materials Please contact us)
2.1.18 Minimum and maximum deposition thickness 15nm and 1um
2.1.19 ALD: Al_2O_3, TiO_2, ZnO Thicknesses <50nm, Substrates 1cmx1cm to 8” wafers
2.1.20 Temperature of upto 400C

2.2 PVD

2.2.1 Sputtering: Metals* upto 300 nm (Process and Material specific, for details Please contact inup.cense@gmail.com) Gold/Platinum/Palladium/Silver up to 200nm, for >200nm Approval needed from concern manager, Please contact inup.cense@gmail.com)

2.2.2 Dilelectrics* of upto 200nm, (>200nm Process and Material specific, Please contact inup.cense@gmail.com)
2.2.3 Sputter Metal: Substrates 1cm x 1cm to 4” wafers loading capacity.
Uniformity in Stationary: 3-4% across 2” (For 7.5 cm Throw distance)
Uniformity in Rotation: 4% across 2” (For 7.5 cm Throw distance)
Substrate Heating of up to 600 deg C
Chamber Heating up to 100 deg C
2.2.4 Sputter Dielectric: Substrates 1cm x 1cm to 4” wafers loading capacity
Substrate/Localized heating of up to 600 deg C
Chamber/Halogen lamp heating up to 100 deg C

2.2.5 Cu, Fe and Zn can be deposited in non-cleanroom environment. Samples with these films are not allowed in cleanroom.

2.2.6 E-Beam evaporation: Metals* up to 250nm (Process specific)
Aluminium coating up to 2 um is feasible
Dielectrics of up to 200nm (Process Specific)

2.2.7 Substrates 1cm x 1cm to 6" wafer loading capacity.
Film Coating with 1-2% uniformity across 4" diameter

3. Etch

3.1 Dry Etch

3.1.1 Dedicated RIEs for Silicon, dielectric ,
and III-V semiconductor, and metals

3.1.2 Gases available in RIEs O_2, Ar, N_2, H_2, Cl_2, BCl_3, CH_4, HBr, SF_6, CHF_3, C_4F_8

3.1.3 Material that can be etched are Si, Ge, SiGe, Oxide, Nitride

3.1.4 Substrates small pieces(1cmx1cm) to 4" wafer

3.1.5 Substrate type- silicon (in case of GaN, sapphire please contact us)

3.1.6 Material strictly not allowed are – PDMS,Cu,SiC,MgO

3.1.7 Dedicated DRIE tool for deep through Silicon etch for MEMS applications

3.1.8 High Aspect ratios and TSV can be made

3.1.9 Only silicon substrates allowed in DRIE

3.1.10 Substrates size: small pieces(1cmx1cm) to 4" wafer

3.1.11 Substrate height: <5mm

3.2 Wet Etch

3.2.1 Wafer cleaning, Silicon, Dielectrics, Metal, CMOS, MEMS processes can be done

3.2.2 CPD and HF vapour etch for stiction free/less structures

3.2.3 Any restrictions? No polymers (including resist), biosamples Materials that would flakes

3.2.4 Fast diffusing (Cu, Zn, Fe, Mn, etc.), toxic metals (Cd, Sb, Se, As, Hg, etc.), their alloys not allowed in clean room due to contamination

4. Inline Characterization

4.1 Ellipsometer: Spectral Range: 245-1000nm
Measurable materials SiO2,Si_3N_4 , PolySi, PolyGe, LTO,a-Si,Al_2O_3, TiO_2,WO_3,CeO_2,Gd_2O_3, MgO, ITO, HfO_2, ZnO
Transparent films up to 10um can be measured.

Opaque films of Thickness <30nm can be measured.
Sample size of 1cmx1cm to 12” wafer

4.2 Dektak: Step height measurement 20nm to 500um

4.3 Curvature profile: Sample size range: 1cmx1cm to 200/300mm diameter

4.4 Four Point Probe: Sheet resistance range: from 0.001 Ω/Square to > 800K Ω/Square, samples of 1cm square to 8inch wafer

4.5 KMOS: Stress and Curvature can be measured

5. (Non Cleanroom) Processes
   - 5.1 Anelva Sputtering: Material* thickness deposition range 5nm to 150nm
   - 5.2 Gases: N2,Ar,O2
   - 5.3 Substrate heating upto 300C
6. Thermal Evaporator
   - 6.1 Materials: Al, Cr, Au, Pd, Ti, Ni, Ag, Ca, Bi, Alq3, MoO3, BCP, CuPc, Al, Ag, LiF, V2O5.
   - 6.2 Thickness: 20nm to 150nm
7. eBeam Evaporator: 4pockets
   - 7.1 Thickness: 10 to 150nm
   - 7.2 Materials: Cr,Ti,Ag,Au,Al, Al_2O_3, ITO
8. RIE Anelva: Ar/O2, CF4, N2
9. Bell Jar Thermal Evaporator
   - 9.1 Materials: Al, Cr, Au, Ag, Bi, V2O5, Alq3, MoO3
   - 9.2 Thickness: 10 to 100nm metals, 5 to 50nm for oxides
   - 9.3 Lindberg Furnace: Temperature up to : 1000°C
     Gases Used : Ar, N2 and O2,
     Quartz tube size : 3”dia,
     Substrate maximum size allowed: 2”
10. Wet Etch: Acids
    - 10.1 Piranha, HF, Copper, Fe and Metals
11. Wet Etch: Solvents
    - 11.1 Actetone, IPA, Lift Off, Sonication
12. Spin Coater: 60 to 8000rpm
    - 12.1 Holding capacity : 4” wafer
13. Lithography MJB3:
    - 13.1 4” Mask Plate
    - 13.2 Substrates upto 3” wafer
    - 13.3 Flood Exposure(single layer only), minimum feature of 5um

14. Sputter Metal Target List

Sputter1 Metals
Aluminum
Chromium
Gold
Molybdenum
Nickel
Platinum
Silver
Titanium
Tungsten
Niobium
Si Undoped

15. Sputter Dielectric Target List

Sputter2 Oxide/Nitride	
Aluminum Oxide	Aluminum Nitride
Cerium Oxide	
Hafnium Oxide	
Indium Tin Oxide	
Silicon Dioxide	
Tantalum Pent oxide	
Titanium Dioxide	
Zinc Oxide	
Aluminum doped Zinc oxide	
Zirconium Oxide	

E-Beam materials list

All materials are in the form of pellets (most of them size around 1 mm to 10 mm)

E-Beam Evaporator
Alumina
Aluminum
Chromium
Germanium Metal
Gold
Indium Tin Oxide
Nickel
Palladium
Platinum
Silicon
Silicon Dioxide
Titanium
Titanium Oxide

Non Clean room Sputter List

Sl. No.	**Materials Name**	**Purity (%)**	**Diameter (mm)**	**Thickness (mm)**
1	Silicon Dioxide (SiO2)	99.999	76.2	6
2	Tungsten Oxide (WO3)	99.95	76.2	6
3	Carbon Graphite (C)	99.995	76.2	5
4	Chromium Oxide (CrO)	99.98	76.2	6
5	Megnesium Oxide (MgO)	99.99	76.2	6
6	Indium Tin Oxide (ITO)	99.99	76.2	6
8	Carbon (C)	99.9	76.2	6
9	Graphite (C)	99.999	76.2	6
Sputter Metal Target List				
7	Germanium (Ge)	99.999	76.2	3
10	Barium Strontium	99.99	76.2	6

11	Silicon Phosphorous (n-type)	99.999	76.2	5
12	Lead Zirconate Titanate (PZT)	99.99	76.2	5
13	Germanium Boron doped (Ge)	99.999	76.2	3
14	Chromium (Cr)	99.9	76.2	6
15	Aluminium (Al)	99.999	76.2	6
16	Iron (Fe)	99.9	76.2	4
17	Nickel (Ni)	99.98	76.2	4
18	Aluminium 1% Silicon	99.999	76.2	5
19	Nickel Iron (Ni Fe)	81 % Ni 19% Fe 99.99	76.2	2
20	Nickel Iron (Ni Fe)	80 % Ni 20% Fe	50	1.5
21	Copper (Cu)	99.999	76.2	6
22	Palladium (Pd)	99.99	76.2	2
23	Titanium (Ti)	99.995	76.2	3
24	Platinum (Pt)	99.99	50	2.5
25	Gold (Au)	99.99	58	3
26	Silver (Ag)	99.99	76.2	2.5
27	Cobalt (C)	99.99	76.2	5
28	Tungsten (W)	99.95	76.2	6
29	Tantalum (Ta)	99.99	76.2	6

16. Wet Etch Material List

Metals: Al, Au, Cr, Ti, Pt, Ni, Hf etc

Dielectrics: Si_3N_4, SiO_2 , Si: KOH, TMAH,

Photo Resist Removal and Lift off processes,

ITO, ZnO, Ge etching,

For more materials please contact us

Electroplating : Gold only, please contact us inup.cense@gmail.com